UCSP - A Wafer-Level Chip-Scale Package

Introduction

The Wafer-Level Chip-Scale Package (WLCSP) is a type of CSP which enables the integrated circuit (IC) to be attached to the printed-circuit board face-down, with the chip's pads connecting to the PC board's pads through individual solder balls without needing any underfill material (Figure 1). This technology differs from other ball-grid array, leaded, and laminate based CSP's because there are no bond wires or interposer connections. The principle advantage of the WLCSP is that the IC-to-PC board inductance is minimized. Secondary benefits are reduction in package size and manufacturing cycle time and enhanced thermal conduction characteristics. Maxim's WLCSP is trademarked as UCSP.

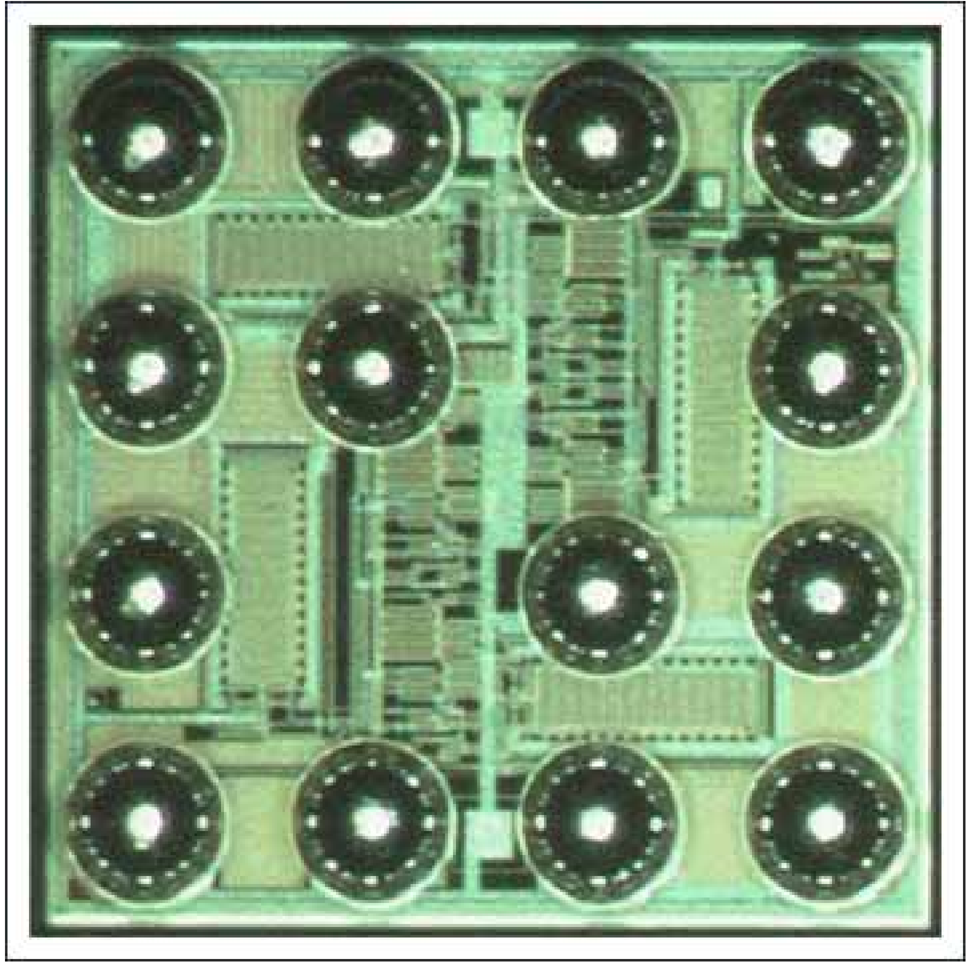


Figure 1. Photo of a 4x4 UCSP, bottom side view

UCSP Construction

Maxim's UCSP structure is manufactured by building-up on a silicon wafer substrate. A film of BCB (Benzocyclobutene) resin is applied over the wafer surface. This film provides mechanical stress relief for the ball attachment and electrical isolation at the die surface. Vias are imaged in the BCB film, providing electrical contact to the IC bond pad. An UBM (Under Ball Metal) layer is added over vias. Typically, a second application of BCB serves as a solder mask to define the diameter and position of reflowed solder balls. The standard solder ball material is eutectic tin-lead, i.e., 63%Sn/37%Pb. A cross section of UCSP structure is shown in Figure 2.

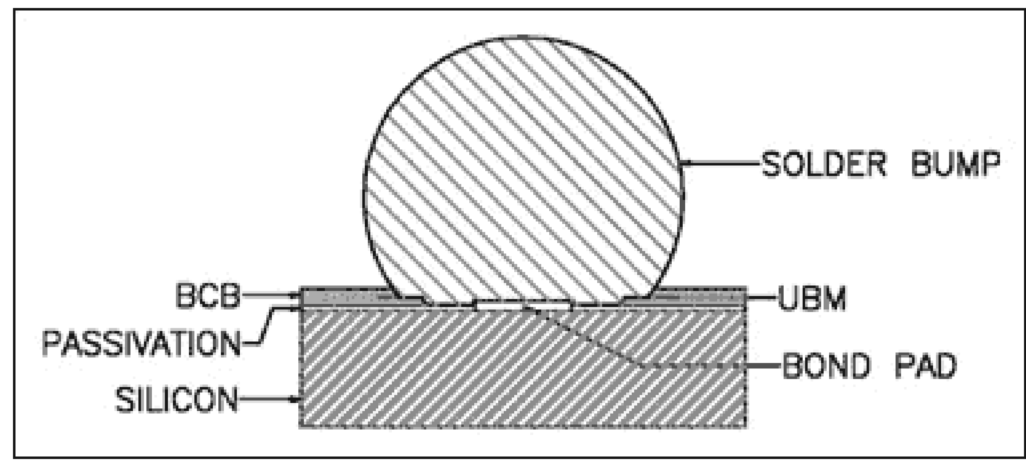


Figure 2. Cross-section diagram of a typical UCSP

UCSP ball arrays are configured based on a rectangular grid with uniform grid pitch. The UCSP ball array may contain any number of rows (ND) and any number of columns (NE) such that $6 \geq ND \geq 2$ and $6 \geq NE \geq 2$. Refer to Table 1 for the basic UCSP configurations, Table 2 for typical dimensions, and Figure 3 for the mechanical symbol conventions cited in Table 2. Depopulation of balls is possible, leading to numerous ball array variations not listed in Table 1.

Table 1. UCSP Configurations

Ball Array*	Die Size in X, mm [mils]	Die Size in Y, mm [mils]
2x2	1.0 [40]	1.0 [40]
3x2	1.5 [60]	1.0 [40]
3x3	1.5 [60]	1.5 [60]
4x3	2.0 [80]	1.5 [60]
4x4	2.0 [80]	2.0 [80]
5x4	2.5 [100]	2.0 [80]
5x5	2.5 [100]	2.5 [100]
6x5	3.0 [120]	2.5 [100]

6x6	3.0 [120]	3.0 [120]

Note: Design of ball array for a particular device may have de-population for less than fully populated ball count. Detailed UCSP drawings are available from Maxim's package outline directory at http://www.maxim-ic.com/cgi-bin/packages.

Table 2. Typical UCSP Dimensions

Item	Millimeters	Inches
Ball Pitch e	0.50 BSC	0.0197 BSC
Ball Diameter øb	0.355 ±0.025	0.014 ±0.001
Silicon Thickness A2	0.330 ±0.025	0.013 ±0.001
Ball Height A1 (before board attach)	0.293 ±0.0125	0.0115 ±0.0005
Total Package Height A (before board attach)	0.623 ±0.040	0.0245 ±0.0016
Mounted Package Height (depends on assembly parameters)	0.65 Typical	0.026 Typical
ND	Number of Rows in Ball Matrix	
NE	Number of Columns in Ball Matrix	
Array Offset SD	SD = 0 if ND is an odd number or SD = 0.25 [0.0098] if ND is an even number	
Array Offset SE	SE = 0 if NE is an odd number or SE = 0.25 [0.0098] if NE is an even number	

Note: Design of ball array for a particular device may have de-population for less than fully populated ball count. Detailed UCSP package drawings are available from Maxim's package outline directory at http://www.maxim-ic.com/cgi-bin/packages.

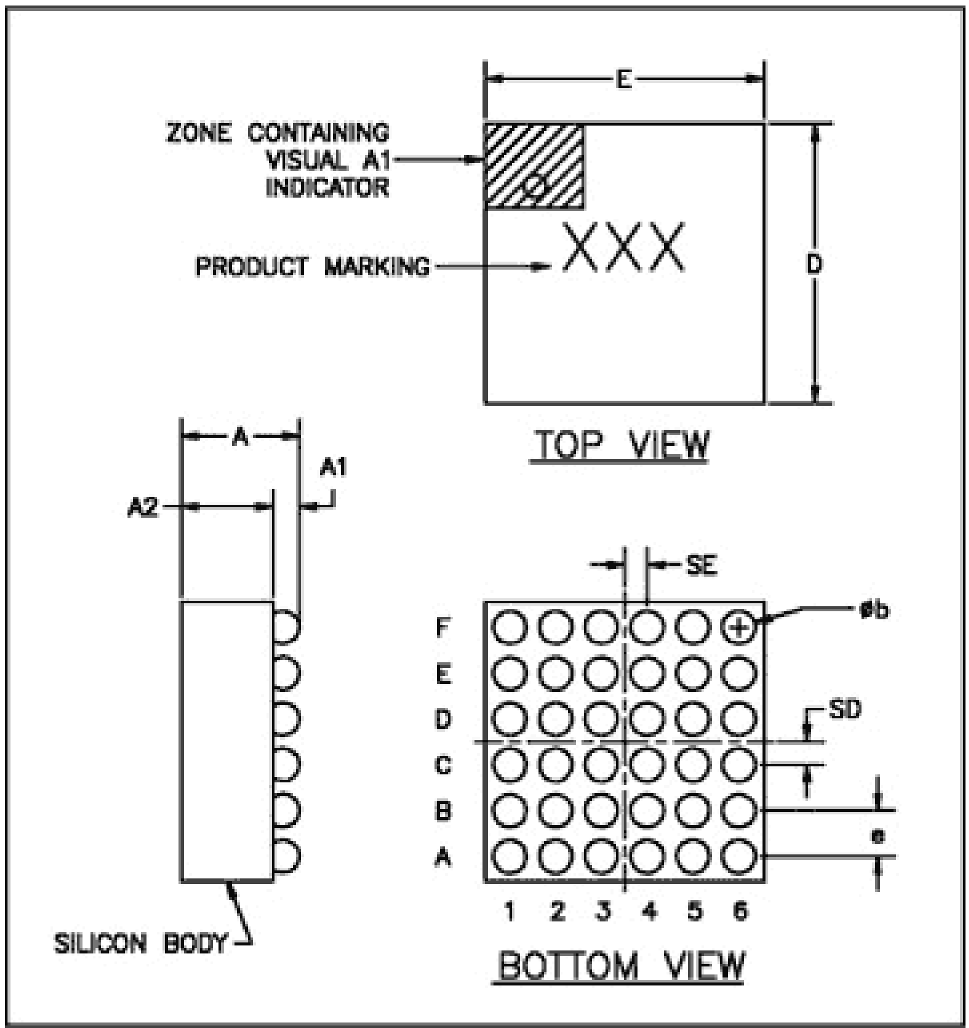


Figure 3. Symbol conventions for UCSP package outline drawing, full 6x6 array

UCSP Carrier Tape

Maxim ships all UCSP's in tape-and-reel (T&R). UCSP tape-and-reel requirements are based on EIA-481 standard. A typical tape-and-reel construction is shown in Figure 4 with key and variable dimensions shown in Table 3.

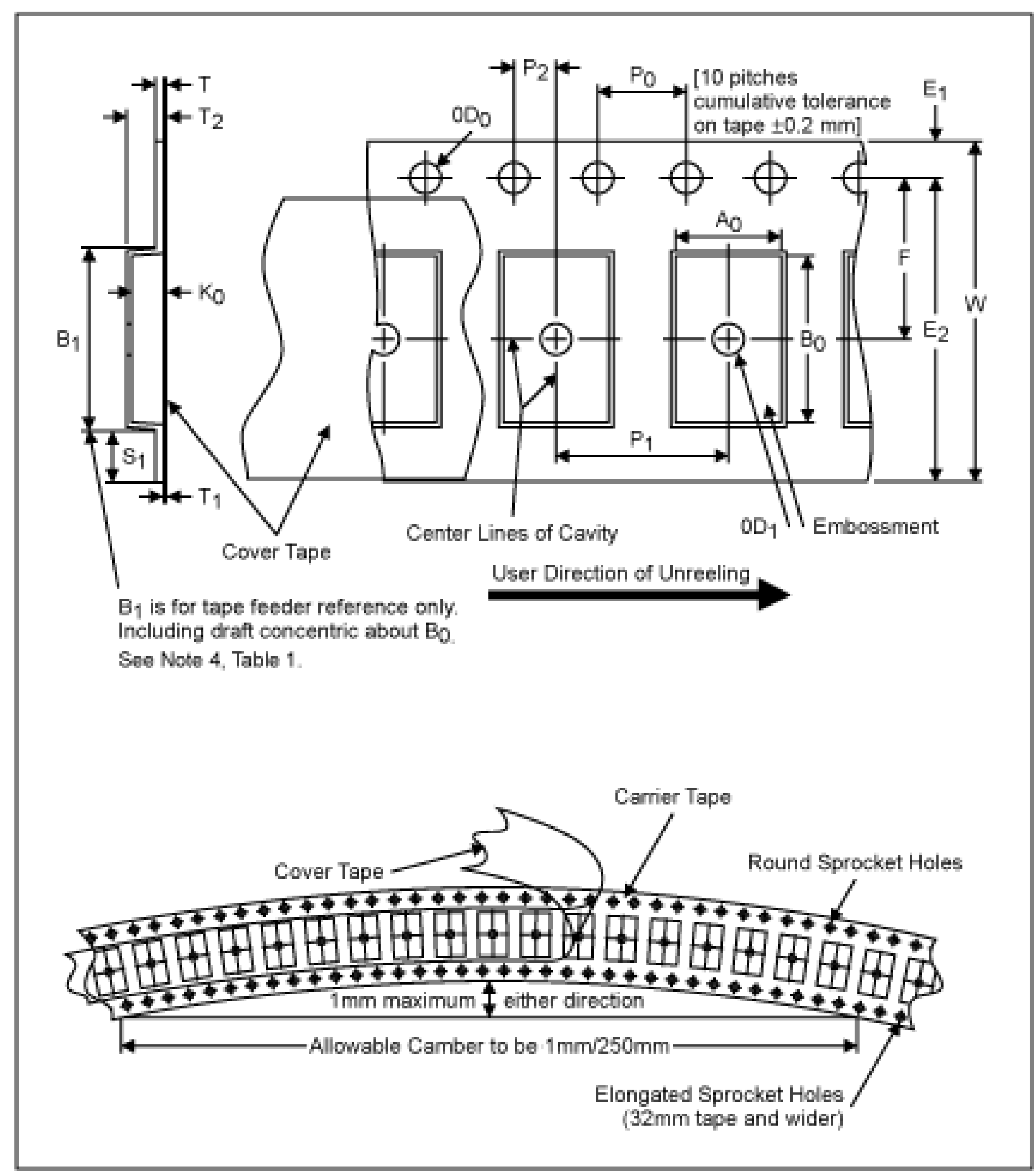


Figure 4. Typical UCSP carrier tape construction

Table 3. Key and Variable Dimensions of UCSP Tape-and-Reel

Key Dimensions (millimeters)								
Tape Size	**D_0**		**E_1**	**P_0**	**P_2**	**T_1 Max**	**G Min**	**R Min (See Note 2)**
8mm	1.5	+0.10 -0.00	1.75 ±0.10	4.0 ±0.10	2.0 ±0.05	0.10	0.75	25
Variable Dimensions (millimeters)								

Tape Size	E_2 Min	F	W Max	P_1 (See Note 4)	A_0, B_0	T
8mm	6.25	3.5 ±0.05	8.3	2.0 ±0.05 or 4.0 ±0.10	See Note 1	1.6mm max

Table 3 Notes

1. The cavity defined by A_0, B_0 and T shown in Figure 4 shall be configured to provide sufficient clearance surrounding the component so that:

- the component does not protrude beyond either surface of the carrier tape;

- the component can be removed from the cavity in a vertical direction without mechanical restriction after the top cover tape has been removed;

- the rotation of the component is limited to ±10° maximum (see Figure 5).

2. Radius R minimum is a mechanical bending radius characteristic of the tape design and materials. Actual reel hub radius must be greater R minimum. Tape with components in normal orientation shall pass around radius R minimum without damage to tape or components. Tape feeders and any other tape handling, shipping, or storage conditions should be configured by user of tape such that actual bending radius is always greater than R minimum.

3. Bar code labeling (if required) shall be on the side of the reel opposite the sprocket holes. Refer to EIA-556.

4. If P_1 = 2.0mm, the tape may not properly index in all tape feeders.

5. Balls are facing down in the tape-and-reel carrier. Pin A1 orientation is consistent in each pocket in the carrier tape. Mark layout will have Pin A1 ID on top left-hand corner. See Figure 6 shown below for details.

6. The cover tape shall have a total peel strength of from 0.1 N to 1.0 N (10 grams to 100 grams calibrated scale reading). The direction of pull shall be opposite the direction of carrier tape travel such that the cover tape makes an angle of between 165 and 180 degrees with the top of the carrier tape. The carrier and/or cover tape shall be pulled with a velocity of 300mm ±10 mm/minute during peeling.

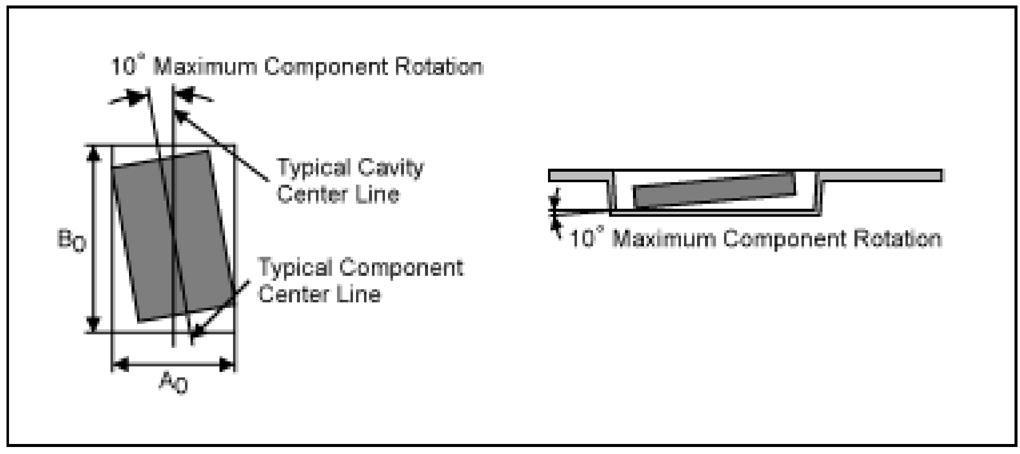


Figure 5. Maximum allowable rotation of UCSP inside tape-and-reel pocket

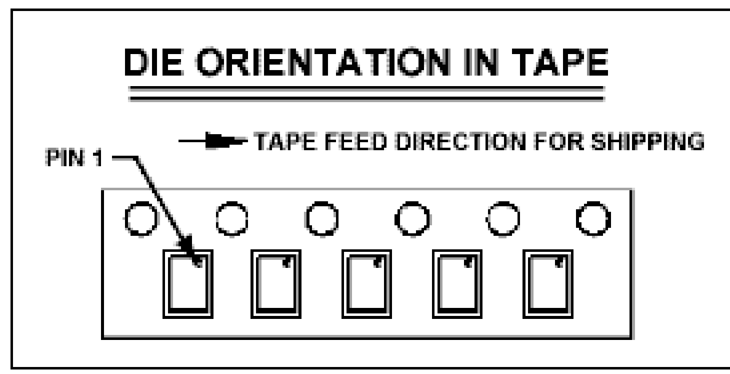


Figure 6. UCSP orientation vs. tape feed direction

Printed-Circuit Board Layout

Successful implementation of UCSP in assembly requires attention to circuit board layout. Printed Circuit Board (PCB) layout and fabrication can affect UCSP assembly yield, device performance, and solder joint reliability. Design guidelines for UCSP land patterns and specifications for PCB fabrication may differ from leaded devices and laminate-based BGA's.

Two types of land patterns are used for surface-mount packages (see Figure 7):

- Solder-Mask Defined (SMD). Pads have solder-mask openings smaller than metal pads. The board designer defines the shape code, position, and nominal size of the pad; actual pad opening size is controlled by the solder-mask fabricator. The solder mask is typically LPI (liquid photoimageable).
- Non-Solder-Mask Defined (NSMD). Metal pads are smaller than solder mask openings. In SMD pads on surface-routed boards, a portion of the printed circuit conductor trace is exposed to solder wetting.

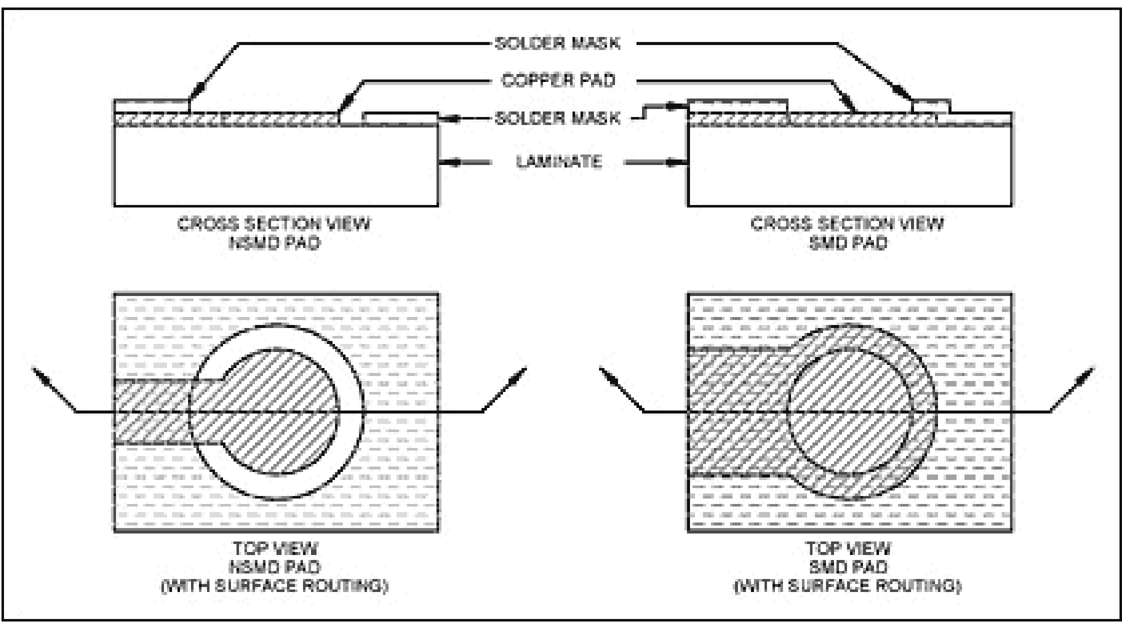


Figure 7. Land pad options: Solder-mask defined (SMD) vs. Non-solder-mask defined (NSMD)

The circuit board designer must choose between NSMD and SMD pads with consideration of the power, ground, and signal routing requirements. Special microvia designs may eliminate surface routing, but require more advanced printed circuit technology. Once selected, the UCSP pad styles on a given land pattern should not be mixed. Pads and connecting traces should be arranged symmetrically to prevent off-center solder wetting forces.

Some considerations for selection of UCSP pad styles are:

- Better control of the copper etch process, as compared to the solder-mask etch process in the SMD pad definition, can make NSMD preferable.
- The SMD pad definition may introduce stress concentration near the solder-mask overlap region that results in solder joints cracking under extreme fatigue conditions.
- Depending on PCB fabrication rules for copper line and space, NSMD pads may provide more room for escape routing on the PCB.
- Larger solder mask opening for NSMD pad as compared to SMD pad provides larger process window for UCSP component terminal placement.
- SMD pads can provide greater width of copper trace for low inductance connections to power or ground planes.
- Maxim used NSMD design during temperature cycle testing.

Typically, the NSMD PCB layout assumes 1/2 or 1 oz. starting copper foil thickness. The NSMD circular copper pad diameter should be 11 +0/-3 mils and NSMD circular solder-mask apertures should be 14 +1/-2 mils. To prevent solder thieving, each NSMD copper pad should be connected by one signal trace neck, the neck width being no more than 1/2 the diameter of its connected NSMD copper pad. This is achievable with minimum 4 mil - 5 mil trace width design. Trace necks should be arranged symmetrically within the component land pattern to prevent component placement shift due to unbalanced wetting forces during solder reflow. To prevent

solder shorting, all copper between adjacent pads must be covered by solder mask. Tolerances of solder mask opening and registration to surface copper layer can be critical and varies between board shops. Width of solder mask web (narrow strip between apertures) should meet PCB fabrication rules to prevent break-out of the solder mask web.

With SMD PCB layout, the surface copper thickness is not critical. SMD solder-mask opening should be 12 mils maximum to prevent collapse of the solder joint height, thereby reducing reliability of the UCSP solder joints. Width of copper land pads should meet PCB fabrication rules for minium space and minimum overlap of solder-mask. When a new PCB fabricator is used, qualification of the solder-mask should be performed to insure that the solder-mask quality and solder joint reliability meets the minimum requirements for the user's application.

For best solder mask adhesion and minimum solder wicking under solder mask edges near solder pads, the board specification should call out solder-mask over bare copper (SMOBC). Solder-mask over plating should be avoided due to unpredictable solder-mask adhesion to the plating and possible undermining of the solder-mask edges by molten solder during surface mount assembly reflow.

Metal finish of the PCB land pads affects both assembly yield and reliability. With respect to land pad finish, the following guidelines should be well noted:

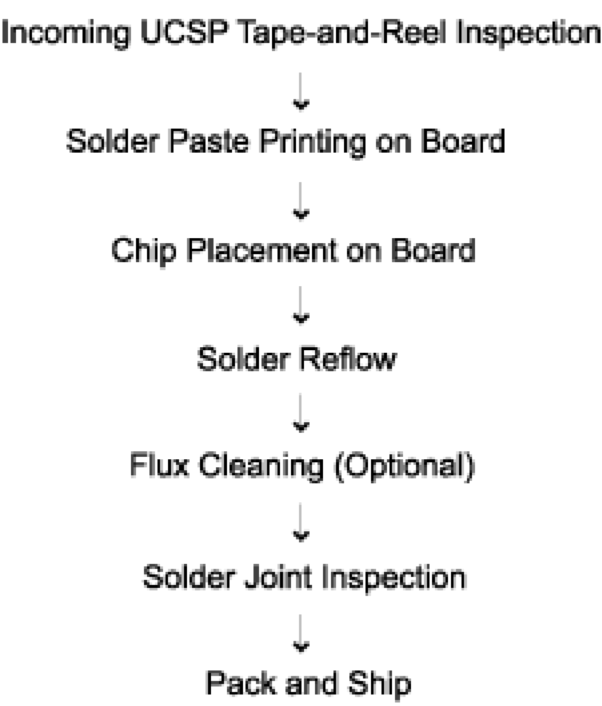
- Copper pads should be finished with organic solderability preservative coating (OSP). OSP is typically less expensive than gold plating and produces the most reliable solder joints.
- Electroless nickel/immersion gold is an acceptable alternative to copper/OSP due to self-limiting gold plating thickness to typically 20 microinches. It is important that the gold thickness must be less than 0.5 micron to avoid making the solder joints brittle, reducing reliability of the solder joint.
- Even if less costly or more readily available than copper OSP or immersion gold, electroplated gold should never be used due to risk of wide process variation in electroplated gold thickness.
- HASL (hot-air solder-level) finish should not be used for UCSP, due to uncontrolled volume and profile of the solder coating.

Maxim recommends solder paste for UCSP assembly. In most PCB layout databases, the layout designer provides Gerber artwork for solder paste stencil. The solder paste aperture layout should then be reviewed by the SMT (surface mount technology) engineer for compatibility with solder paste printing process. By attention to solder paste aperture layout, the PCB designer can help optimize assembly yield. For certain small UCSP with limited ball array size, namely 2x2, 3x2, and 3x3, to minimize solder shorting, good practice is to offset solder paste depositions from the UCSP ball positions by 0.05mm, increasing the stencil aperture pitches from 0.50mm to 0.55mm, up to 0.60mm pitch for 2x2 array (see Figure 8 for detail dimensions). No change is needed to the land pads and solder-mask apertures. For larger ball array sizes (i.e., 4x3, 4x4, 5x4, and greater) peripheral rows and columns of solder paste apertures may be

offset. Where applicable, internal (non-peripheral) paste aperture depositions may be offset toward any de-populated grid array nodes.

SMT Process Flow

A typical UCSP surface mount assembly process flow is shown below followed by guidelines for solder paste printing, component placement, solder reflow, rework of UCSP, pack and ship.



Solder Paste Printing Process

Solder paste printing is the most critical process related to PCB assembly yield. Inspection for paste height, percent pad coverage, and registration accuracy to solderable land patterns is mandatory.

- Solder paste selection: It should be a Sn63/Pb37 eutectic alloy Type 3 (25 to 45 micron solder sphere particle size) or Type 4 (20 to 38 microns), depending on solder stencil aperture size limitations. It is recommended that a low halide (<100 PPM halides) no-clean rosin/resin flux system, J-STD-004 designation ROL0/REL0, be used to eliminate post-reflow assembly cleaning operations.
- Solder Stencil Fabrication: Use laser cut stainless steel foil with electro-polishing or Nickel base metal electroformed foil processes. The Nickel E-form process is more expensive but offers the most repeatable solder paste deposition from ultra small apertures, and has the advantage of being formed to any customer required stencil thickness. Stencil openings with trapezoidal cross section improve paste release from the stencil.
- Solder Stencil Aperture Design: Whenever possible, offset apertures from land pads to

maximize separation between paste deposits and minimize possibility of bridging for UCSP packages with less than 10 ball grid-array patterns (2x2, 3x2, 3x3). Refer to Figure 8 and Table 4 for recommended stencil aperture design parameters.

- Aperture area ratio is defined as the aperture opening area divided by the aperture side-wall surface area. Area ratio of $\geq$ 0.66 with square (25 micron corner radius) vs. round aperture is preferred for solder paste print process repeatability. Area ratio can be increased by using larger aperture or thinner stencil foil.

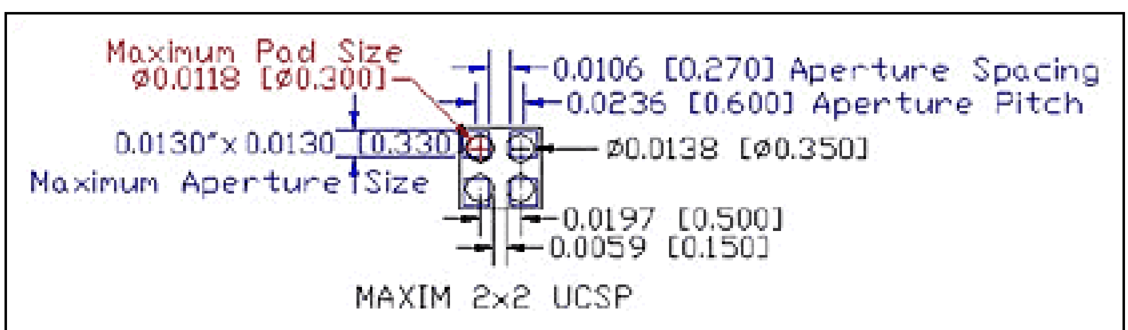


Figure 8. Example of a 2x2 ball grid-array apertures offsets design

Table 4. Recommended Solder Paste Stencil Aperture Designs

Parameters		4x3 through 6x6 Full Ball Arrays		2x2, 3x2, and 3x3 Full Ball Arrays and 4x3 through 6x6 Perimeter-Only Ball Arrays
	Paste Rule Option	A[1]	B	C
	X & Y Paste Aperture Offset[2]	No offset	Inner apertures: 0 (no offset) Perimeter apertures: up to 0.030mm from ball centers	All apertures: up to 0.05mm from ball centers

	Paste Aperture Size	0.305mm square	0.305mm square	0.33mm square
	Stencil Thickness	0.10mm	0.10mm	0.125mm
	Area Ratio[3]	0.76	0.76	0.66
	Comment	Thin stencil	Thin stencil	Tolerates lower placement accuracy

Notes:

1. Maxim UCSP Product Qualification used paste rules Option A.
2. Paste Aperture at center position of ball grid array (0,0) is not offset.
3. Area ratio is defined as the aperture opening area divided by the aperture side-wall surface area. Area ratio of ≥ 0.66 with square (25 micron corner radius) versus round aperture is preferred for solder paste print process repeatability.

Component Placement

UCSPs can be picked up from pocketed carrier tape reels and placed onto PCB substrates using standard automated fine-pitch IC Pick & Place machines with ≤ 0.050mm placement accuracy at 4 sigma. Stationary Tape & Reel feeder bases are also required for all Pick & Place systems. Systems using mechanical centering devices are not acceptable due to the high potential for mechanical damage to the UCSP package.

- The placement accuracy of the Pick & Place system is dependent on its vision alignment of Package Outline centering vs. Ball Grid-Array centering. Package Outline centering is employed for higher speed placement with reduced alignment accuracy requirements and Ball Grid-Array centering is employed for maximum alignment accuracy at lower placement rates. The maximum Package Outline centroid X,Y variation from Ball Grid-Array centroid position is ± 0.035mm.
- The maximum allowable solder ball placement offset from PCB pad center to assure self-centering alignment from solder reflow wetting forces is ± 0.150 mm in X and Y directions.
- All UCSP package contact forces should be controlled to ≤ 5 Newton. It is recommended that the component solder ball Z height placement not exceed 50% of the solder paste height.
- 2D transmission X-Ray inspection is required for placement accuracy verification and measurement.
- The pick and place operation may also require adequate cleaning of pick up nozzles/tips for consistent and reliable picking die from carrier tape and placing die onto the PCB substrate. The following guidelines are recommended for this purpose:

- Clean the die pickup tips with IPA or methanol frequently during pick and place operation. The frequency can be determined by inspecting tips for any foreign matter after several picks and arrive at optimum number of pick intervals.
- Use a pick-up tip that does not touch the laser mark area.
- Use a larger vacuum tip to release the die more consistently and to avoid die misalignment after placement.

Solder Paste Reflow

The Maxim UCSP is compatible with all industry standard solder reflow processes. Nitrogen inert atmosphere reflow soldering is optional.

- Forced gas convection reflow ovens are recommended for controlled heat transfer rates throughout the process.
- Nominal peak temperature is 220° C ±15° C with time above the melting point of solder at 60 sec. ±15 sec., and should be verified at machine setup by inline thermocouple measurements oven profiling. A typical reflow temperature profile for eutectic solder based UCSP is shown in Figure 9.
- UCSP packages are qualified for up to three reflow cycles (at +235° C peak temperature).
- 2D Transmission X-Ray or X-Ray Laminography is recommended as a post-reflow solder joint inspection sample monitoring method for solder shorts, insufficient solder, voids, and potential solder opens.

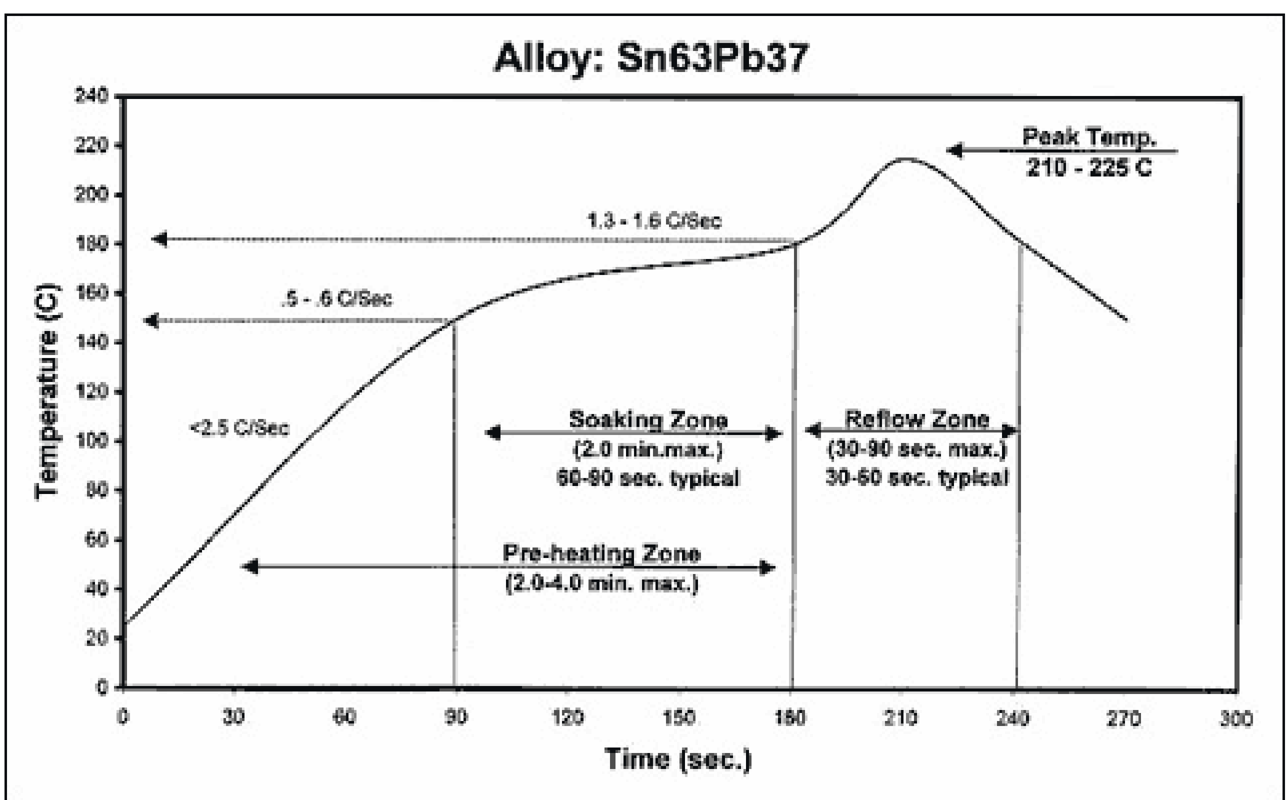


Figure 9. Typical reflow temperature profile for eutectic solder based UCSP

Rework of UCSP

UCSP rework utilizes the same process as for reworking a typical ball-grid array (BGA).

- UCSP removal uses localized heating comparable to the original reflow profile, employing a hot gas convection chimney nozzle and bottom-side preheat.
- Once the nozzle temperature achieves 190° C, the defective UCSP can be removed using plastic tweezers or vacuum tool.
- The PCB pads must be resurfaced using a temperature-controlled soldering iron.
- Gel or tacky flux is then applied to the pads.
- A replacement part is picked up with a vacuum needle pick-up tool and accurately placed using a vision alignment placement jig.
- Reflow the part using the same hot gas convection nozzle and bottom-side preheat, to the original reflow profile.

Pack and Ship

To prevent damage to the UCSP package, care must be taken in packing and shipping UCSP assemblies, especially when the UCSP is mounted without underfill. The packing specification for PCB mounted with UCSP must be reviewed and optimized.

Maxim UCSP Reliability Data

The Maxim UCSP package has been subjected to environmental stress tests similar to the end-user applications. The component-level (or wafer-level) tests such as temperature cycling, pressure pot, and high temperature storage life test have been applied to UCSP products. In addition, the board-level tests such as high temperature operating life, temperature and humidity biased, and temperature cycling have also been performed with UCSP parts mounted on FR4 boards. See Table 5 shown below for detailed test conditions.

Table 5. UCSP Product Reliability Test Conditions

Component-Level Tests

Reliability Test	Test Conditions
Temperature Cycling Test (TCT)	-40° C to +125° C, 1000 cycles, ramp rate 11 ° C/minute, dwell = 15 minutes, one cycle/hour
Pressure Pot Test (PPT)	121° C/100% relative humidity, 15 psig, no bias, 168 hours
High Temperature Storage Life Test (HSTL)	150° C/1000 hours, no bias

Board-Level Tests (with UCSPs mounted on 0.035" thick FR4 boards)

Reliability Test	Test Conditions
High Temperature Operating Life Test (HTOL)	135 ° C ambient, with bias, 1000 hrs
Temperature and Humidity Biased Test (THB)	85 ° C, 85% relative humidity, with bias, 1000 hrs
Temperature Cycling Test (TCT)	-40° C to +125° C, 1000 cycles, ramp rate 11 ° C/minute, dwell = 15 minutes, one cycle/hour

UCSP Reliability Test Results

Reliability test results of Maxim UCSP products are shown in Table 6 which consists of test results for UCSP products with an array size ranging from 3x3 to 5x5.

Table 6. UCSP Product Reliability Test Results

Component-Level Test Results

UCSP Solder Ball Matrix	Part Type	TCT	PPT	HTSL
3x3	MAX1819EBL	0/89	0/89	0/89
3x3	MAX1819EBL	0/91	0/91	0/91

3x3	MAX2246EBL	0/126		0/118
3x3	MAX2246EBL	0/124	1/110[1]	0/105
3x4	MAX4685EBC	0/107	0/107	0/98
4x4	MAX2251EBE	0/86	0/80	0/102
5x5	MAX2291EBA	0/80	1/80[2]	0/80
5x5	MAX2291EBA	0/80	0/80	0/80
5x5	MAX2291EBA	1/80[3]	0/80	0/80

Board-Level Test Results (with UCSPs mounted on 0.035" thick FR4 boards)

UCSP Solder Ball Matrix	Part Type	HTOL	THB	TCT
3x3	MAX1819EBL	0/40	0/41	0/45
4x4	MAX2251EBE			0/45

Table 6 Notes

1. Marginal leakage failure. Cause was unknown. One failure still met the acceptance criteria.
2. Marginal leakage failure. Cause was unknown. One failure still met the acceptance criteria.
3. High value of Icc and Ishdn. Cause was unknown. One failure still met the acceptance criteria.

Additional UCSP Reliability Tests

Maxim has performed UCSP reliability tests with different test conditions as those described in Table 5 and 6. These tests include high-temperature operating life test, temperature humidity bias test, low-temperature operating life test, low-temperature storage life test, and temperature cycling test. Table 7 summarizes the reliability test results from the tests performed on 3x3 UCSP packages. Tests were conducted with UCSP parts mounted on 4-layer FR4 boards. Each assembled FR4 board was then subjected to stress tests as described below. The test results again demonstrated that the Maxim 3x3 UCSP packages could pass all of the tests listed in Table 7.

Table 7. Additional UCSP Reliability Test Results (with UCSP's mounted on 0.062" thick FR4 boards)

Reliability Test	Test Conditions	Test Duration	Results
Temperature Humidity Bias Test	20° C to 60° C, 6 hrs High/6 hrs Low, 90 to 95% R.H., with bias	240 hrs	0/10
High Temperature Operating Life	+70° C ambient, with bias	240 hrs	0/10

Low Temperature Operating Life	-10° C, with bias	24 hrs	0/10
Low Temperature Storage Life	-20° C, no bias	240 hrs	0/10
Temperature Cycling	-35° C to +85° C, 15 min dwell	150 cycles	0/10

Board-Level UCSP Package Reliability (Solder Joint Reliability)

In addition to the standard reliability tests described above, Maxim also performed solder-joint reliability tests on UCSP packages. A temperature cycling test is typically used to determine the reliability of solder joint. Maxim used UCSP with daisy-chain structure, mounted on a 4-layer FR4 board (0.062in thick). The entire board assemblies were tested using temperature cycling chamber with a temperature profile of -40° C to +125° C (1 cycle/hr, 15 minutes ramp, 15 minutes dwell). The resistance measurements were taken on a daily basis. Any resistance reading with increase greater than 10% was considered as a failure. The test results are shown in the below table.

Table 8. Maxim UCSP Solder Joint Reliability Test Results

UCSP MATRIX	TEST CONDITION	CYCLES							
		200	500	1000	1152	1200	1248	1296	1346
6x6 UCSP Daisy Chain (62 mils FR4)	-40° C to +125° C	0/50	0/50	0/50	0/50	0/50	0/50	0/50	0/50

The test results shown in Table 8 demonstrate that Maxim's 6x6 UCSP solder ball joints could pass 1346 cycles, under -40° C to +125° C (1 cycle/hr) conditions without failures.

February 2003

More Information

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